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10/780,157	02/17/2004	Monji G. Jabori	200314182-1	1267

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EXAMINER	
RIAD, AMINE	

ART UNIT	PAPER NUMBER
2113	

DATE MAILED: 07/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/780,157	JABORI, MONJI G.	
	Examiner	Art Unit	
	Amine Riad	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *12* is/are allowed.

6)☒ Claim(s) *1,7-11,13,14,18,21-23 and 25-30* is/are rejected.

7)☒ Claim(s) *2-6,15-17,19,20 and 24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 February 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

Claims 1-30 have been presented for examination.

Claims 1, 7-11,13,14, 18, 21, 22, 23, and 25-30 have been rejected.

Claims 2-6, 15-17,19, 20, and 24 have been objected to.

Claim 12 has been allowed.

Objection

Claim 18 recites "The method of claim 14, where configuring the hardware analyzer includes **or more**" it appears that the word one is missing. Correction is highly suggested.

Claim 22 recites "(Configuring a hardware analyzer where) configuring the hardware analyzer includes **or more**" it appears that the word one is missing. Correction is highly suggested.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 22, 28, and 29 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.
Claims 22, 28, and 29 are not limited to tangible embodiments. In view of applicant's disclosure [specification page 5; line 20], the computer readable medium is not limited to tangible embodiments, instead being defined as including both tangible embodiment for example [solid-state memories, optical and magnetic disks] and intangible

embodiments for example [carrier wave signals]. As such, the claims are not limited to statutory subject matter and are therefore non-statutory.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 7-11,13,14, 18, 21, 22, 23, and 25-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Garrett US Patent 6,018,809.

In regard to claims 1, 13, 23, 28, 29, and 30

Garrett discloses a correlating debugger, comprising:

- First logic configured to receive a first data set from a hardware analyzer that is configurable to analyze a hardware device; (Figure 2; item 38 of figure 3 within trace engine 28) [Examiner considers data collected from the SCSI as hardware data]
- Second logic configured to receive a second data set from a software analyzer that is configurable to analyze a software component; (Figure 2; item 38 of figure 3 within trace engine 28) [Examiner considers data collected from the SCSI as software data]
- Third logic configured to receive a binding data from the hardware analyzer or the software analyzer, where the binding data facilitates synchronizing the first

data set and the second data set;(Figure 2; item 38 of figure 3 within trace engine 28) & (Column 3; lines 19-21) [Each trace engine clock is synchronized with the other trace engine clocks so that all the data collected is synchronized]

- Fourth logic operably connected to the first logic and the second logic, the fourth logic being configured to; receive a signal that indicates that an interaction between the hardware device and the software component has occurred; and upon receiving the signal, to selectively store elements of the first data set and the second data set in a time-ordered data set regard to claim 5 and 6,

Garrett discloses in (Column 1;lines 29-30) that the data collected is commands, status, and messages. Examiner considers the messages as hardware identifier, and commands as application.

In regard to claim 7,

Garrett discloses the correlating debugger of claim 1, where the signal comprises a non-maskable interrupt. (Column 4; lines 37-40)

In regard to claim 8,

Garrett discloses the correlating debugger of claim 1, where the time-ordered data set includes one or more first elements of the first data set and one or more second elements of the second data set, where the first elements are arranged together with the second elements in order based on time. (Column 3;lines 23-24)

In regard to claim 9,

Garrett discloses the correlating debugger of claim 1, where the software component is configured to run on a first processor and a processor executable instructions associated with the first logic, the second logic, the third logic, or the fourth logic are configured to run on a second processor. (Column 3; lines 20-22)[Examiner points out that trace engines are located between the host and the storage system. Examiner considers that first processor belongs to the host, and the second processor belongs to the storage system in this case]

In regard to claim 10,

Garrett discloses the correlating debugger of claim 1, where the software component and processor executable instructions associated with one or more of, the first logic, the second logic, the third logic, and the fourth logic are configured to run on a first processor. (Figure 3; item 32) & (Column 3;lines 10-12)

In regard to claim 11,

Garrett discloses the correlating debugger of claim 1, where the software analyzer comprises a kernel debugger. (Column 4;line 26) [The IPC-6500 disclosed comprises a kernel by reference]

In regard to claim 14

Garrett discloses a method, comprising:

- Establishing a relationship in a debugger between a hardware device and a software component that will perform a software operation related to the hardware device; (Figure 2; item 38 of figure 3 within trace engine 28) & (Column 3; lines 19-21) [Each trace engine clock is synchronized with the other trace engine clocks so that all the data collected is synchronized]
- Configuring a software analyzer to collect a first data set related to the software component as the software component performs the software operation and to cause the first data set to be delivered to the debugger; [Examiner considers data collected from the SCSI as software data]
- Configuring a hardware analyzer to collect a second data set related to the hardware device as the hardware device performs a hardware operation and to cause the second data set to be delivered to the debugger; (Figure 2; item 38 of figure 3 within trace engine 28) [Examiner considers data collected from the SCSI as hardware data]
- Detecting a first event that signals a beginning of the software operation and controlling the software analyzer to begin delivering the first data set to the debugger; (Column 4;lines 40-44)[Examiner points out the interrupt is used for both the hardware and the software]
- Detecting a second event that signals a beginning of the hardware operation (Column 4;lines 40-44)[Examiner points out the interrupt is used for both the hardware and the software]

- controlling the hardware analyzer to begin delivering the second data set to the debugger; and selectively storing together, in order, elements of the first data set and elements of the second data set, where the order is based, at least in part, on the time at which an event associated with generating an element occurred. (Figure 2; item 38 of figure 3 within trace engine 28) & (Column 3; lines 21-23)

In regard to claim 18,

Garrett discloses the method of claim 14, where configuring the hardware analyzer includes or more of, identifying one or more types of data available in the hardware device to be reported on by the hardware analyzer, and identifying one or more types of events from the hardware device to be reported on by the hardware analyzer.(Garrett discloses that data collected is commands, status , and message information in the background of the invention. Examiner considers this disclosure as an identification)

In regard to claim 21,

Garrett discloses the method of claim 14, where selectively storing together elements of the first data set and elements of the second data set includes selectively adding an element of the second data set to the first data set. (Figure 2; item 38 of figure 3 within trace engine 28) & (Column 3; lines 21-23) [Since the system contains many trace engines it is inherent to add second data to the already stored first data]

In regard to claim 25,

Garret discloses the method of claim 23, where binding the hardware analyzer to the software analyzer includes establishing a logic connection in a correlating debugger configured to receive data from the hardware analyzer and the software analyzer.(Column 3;lines 19-20)[Synchronizing each trace engine's clock necessities a logic connection]

In regard to claim 26,

Garrett discloses the method of claim 23, where binding the hardware analyzer to the software analyzer includes establishing a physical connection at a correlating debugger configured to receive data from the hardware analyzer and the software analyzer. (Column 3; lines 22-23) [All trace engines send data to be stored, and finally read by the debugger CPU here]

In regard to claim 27,

Garrett discloses in a computer system having a graphical user interface comprising a display and a selection device, a method of providing and selecting from a set of data entries on the display, the method comprising (Column 4; lines 26) [The IPC included here by reference includes all this features]:

- Retrieving a set of data entries, where a data entry represents an operation associated with ordering data received from a hardware analyzer configured to analyze a hardware device and a software debugger configured to analyze a device driver configured to perform one or more of, (Figure 2; item 38 of figure 3

within trace engine 28) [Examiner considers data collected from the SCSI as hardware and software data]

- Servicing interrupts from the hardware device, polling the hardware device and polling a bus by which the piece of computer hardware and the software debugger are operably connected; (Column 4; lines 40-44)
- displaying the set of data entries on the display;(Column 4; line 25-26) [This analyzer includes the claimed feature]
- Receiving a data entry selection signal indicative of the selection device selecting a selected data entry; and in response to the data entry selection signal, initiating an operation associated with the selected data entry. (Column 4; lines 54-58)

Allowable Subject Matter

Claims 2-6, 15-17,19, 20, and 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 12 has been allowed.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant s invention. U.S. Patent 5,555,419 pertains to correlating data, but lacks the hardware part of data collection. See PTO 892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Amine Riad whose telephone number is 571-272-8185. The examiner can normally be reached on 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on 571-272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AR
Amine Riad
Patent Examiner
7/8/2006